

FORM PTO-1449 (Modified)	Attorney Docket No.: 103-1	Application No.: 09/577,238
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	Applicant: YING-WAI, Ho et al.	
	Filing Date: May 23, 2000	Group: 2193

Reference Designation **U.S. PATENT DOCUMENTS** Page 1

Examiner Initial	Document No.	Date	Name	Class	Sub-class	Filing Date (if Appropriate)
<u>CD</u> AA	5,862,066	1/19/99	Rossin et al	364	736	
<u>CD</u> AB	6,298,365	10/2/01	Dubey et al	708	495	
<u>CD</u> AC	6,401,108	6/4/02	Van Nguyen	708	671	
<u>CD</u> AD	6,581,087	6/17/03	Inoue et al	708	671	
<u>CD</u> AE	5,619,198	4/8/97	Blackham et al	341	150	
<u>CD</u> AF	6,175,907	1/16/01	Elliott et al	712	1	
<u>CD</u> AG	5,977,987	11/2/99	Duluk, Jr.	345	441	
<u>CD</u> AH	5,982,380	11/9/99	Inoue et al	345	434	
<u>CD</u> AI	6,631,392	10/7/03	Jiang et a	708	498	
<u>CD</u> AJ	6,697,832	2/24/04	Kelley et al	708	501	
<u>CD</u> AK	6,714,197	3/30/04	Thekkath et al	345	427	
<u>CD</u> AL	6,732,259	5/4/04	Thekkath et al	712	233	

FOREIGN PATENT DOCUMENTS

Document No.	Date	Country	Class	Sub-class	Translation (Yes/No)

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

<u>CD</u> AM	"MIPS Extension for Digital Media with 3D," MIPS Technologies, Inc., pp. 1-26, Dec 27, 1996.
<u>CD</u> AN	Thekkath et al, "An Architecture Extension for Efficient Geometry Processing," pp. 1-23, Presented at Hot Chips 11, A Symposium of High-Performance Chips, Stanford Univ. (August 1999) (submitted for conference review July 14, 1999)
<u>CD</u> AO	Uhler, M., "Optimizing Game Applications for the MIPS RISC Architecture," 1999 Computer Game Developer's Conference, San Jose, CA, 14 pages (March 1999) (submitted for conference review on 2/12/99)
<u>CD</u> AP	Uhler, M., "Optimizing Game Applications for the MIPS RISC Architecture," 1999 Computer Game Developer's Conference, San Jose, CA, slides 1-22 (March 1999)
<u>CD</u> AQ	Kubosawa, H. et al., "A 2.5-GFLOPS, 6.5 Million Polygons per Second, Four-Way VLIW Geometry Processor with SIMD Instructions and a Software Bypass Mechanism," IEEE Journal of Solid-State Circuits, IEEE, Vol. 34, No. 11, pp. 1619-1626, (November 1999) (appears to correspond to document AR1, Higaki, N. et al.).
<u>CD</u> AR	Rice et al, "Multiprecision Division on an 8-Bit Processor," Computer Arithmetic, 1997 (Proceedings, 13th IEEE Symposium on July 6-9, 1997, pp. 74-81)
<u>CD</u> AS	Oberman et al., "AMD 3DNow! Technology and the K6-2 Microprocessor" (presentation), Proceeding Notebook for Hot Chips 10, August 16-18, 1998 (pp. 245-254).
<u>CD</u> AT	U.S. Patent Application Serial No. 09/364,512, "Processor with Improved Accuracy for Multiply-Add Operations," Ying-wai Ho et al, filed on July 30, 1999
<u>CD</u> AU	U.S. Patent Application Serial No. 09/363,637, "System and Method for Improving the Accuracy of Reciprocal and Reciprocal Square Root Operations Performed by a Floating-Point Unit," by Ying-wai Ho et al, filed on July 30, 1999
<u>CD</u> AV	U.S. Patent Application Serial No. 09/364,786, entitled "Processor Having a Compare Extension of an Instruction Set Architecture," by Radhika Thekkath et al, filed on July 30, 1999

EXAMINER [Signature] DATE CONSIDERED 05/13/05

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

